REMARKS

Claims 1-30 are present in this application. Claims 8-11 and 21-24 have been withdrawn. Applicants reserve the right to present such claims at a later time in a divisional application. Claims 1 and 12-14 are independent claims.

Claim Rejection under 35 USC 103 – Chan, Sung

Claims 1-7, 12-20, and 25-30 have been rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Application Publication 2003/0005214 (Chan) in view of U.S. Application Publication 2002/0130356 (Sung). Applicants respectfully traverse this rejection.

Claim 1

Claim 1 will be argued as a representative claim. The other independent claims 12-14 recite the features of claim 1, plus additional features.

Embodiments covered by claim 1 are directed to a semiconductor memory device (e.g., Fig. 20, semiconductor memory device 11; Fig. 22, memory device 12 or 13; Fig. 23; Fig. 24; Fig. 25, memory device 16). The semiconductor memory device includes a nonvolatile memory section (e.g., 302, 305, 21, 316) anda volatile memory section (e.g., 303, 306, 22, 317).

The nonvolatile memory section includes a nonvolatile memory cell (e.g., Figs. 1, 2, 8, 13-18) having a single gate electrode (e.g., 104, 217) formed on a semiconductor layer (e.g. 101) via a gate insulating film (e.g., 103), a channel region (area under gate insulating film) disposed under the gate electrode, diffusion regions (e.g., 107a, 107b) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (e.g., 131a, 131b) formed on both sides of the gate electrode and having a function for retaining charges. Each of the memory functional units are an insulator film (e.g., specification at page 28, lines 9-12).

As disclosed in the present specification it is preferable that a memory cell satisfies the requirements that (3) an insulator retains charges in the memory functional unit, as well as (9) there being no electrode for assisting the writing/erasing operation on the memory function unit (see page 27, lines 12-22). In the case where the memory functional units are made of an insulator, it becomes unnecessary to make the memory function unit independent for each

memory cell. Subsequently, the margin between neighboring memory cells can be reduced. In particular, the area occupied by a memory cell can be reduced to less than the case where the charge retaining area in the memory functional unit is made of a conductor (for example, polysilicon film) (para. bridging pages 28-29).

Sung

Sung discloses a need to create a memory cell that is easy to reduce in size, has multiple storage capacity and requires proportionally small program current. Sung discloses that such a goal of increased density leads to a problem of potential for misalignment that occurs in split gate flash memories. Sung discloses that a solution to this problem can be an arrangement having a plurality of floating gates with self alignment, that includes source and drain areas that are a portion of buried bit lines, and a control gate that extends beyond the cell to form a word line. (see paragraph 0006).

Sung discloses an arrangement wherein "polysilicon sidewalls are used as floating gates for a flash memory." In the arrangement, "the sidewalls partially extend over ion implanted bit lines that operate as sources and drains." Furthermore, Sung discloses "Polysilicon control gates are formed over the sidewalls in an orthogonal orientation extending the length of the word line." (paragraph 0007; see Fig. 2a).

Figures 1f, 2a, and 2b are views of Sung's final product. Figs. 2a and 2b show a plurality of polysilicon control gates 32 extending the length of a word line of the flash memory and deposited over an ONO coating 18 and orthogonal to the plurality of polysilicon sidewalls represented by 30, 35, 36, 37, and 38 (paragraph 0020). Bit line 33 is shown under a portion of polysilicon sidewall 36 and polysilicon sidewall 35 where two sidewalls are located on opposite sides of the buried bit line 33. Similarly, a bit line 34 is shown under a portion of polysilicon sidewall 37 and polysilicon sidewall 38.

Chan

Chan discloses that it is known to combine a Flash memory and SRAM in the same package module, such as a ball grid array (para. 0006).

Differences over Chan and Sung

The Office Action relies on Sung for teaching features of the claimed nonvolatile memory cell. In particular, the Office Action alleges that Sung teaches a nonvolatile memory cell including charge storage areas (15) on both sides of a single gate electrode (control gate 19 at void 17), a gate insulating film (11), a channel region, diffusion regions (14), and memory function units (15).

Applicants disagree that Sung teaches the claimed "single gate electrode" within the context of a nonvolatile memory cell.

As noted above, Sung teaches a memory cell having a split gate arrangement on each sidewall of the control gate (para. 0007). In particular, Sung teaches that: "The polysilicon sidewall 36 forms the split gate flash memory cell (2') and the polysilicon sidewall 35 forms the split gate flash memory cell (1)" (para. 0021). Thus, Applicants submit that Sung does not teach at least the claimed "single gate electrode."

In addition, contrary to the present invention, Sung discloses polysilicon (i.e., conductor) memory cells. In the present invention, each of the memory function units is an insulator film.

In the rejection of claims 29 and 30, the Office Action alleges that the ONO layer 18 and insulating film 11 constitute part of the memory function unit. Thus, the claims have been amended to clarify that the memory function unit of the present invention, particularly the part that retains charge, is an insulator.

Applicants submit that Sung fails to teach the claimed structure for a nonvolatile memory cell. As mentioned above, the present invention offers an advantage that the area occupied by a memory cell can be reduced to less than an arrangement where the charge retaining area in the memory functional unit is made of a conductor (e.g., polysilicon film as in Sung; present specification at paragraph bridging pages 28-29).

With respect to claim 3, the Office Action appears to interpret the claimed "chip." in a manner that was not intended. In order to clarify the intended meaning of "chip," the claim has been amended to indicate that the chip has a single common substrate (e.g., see Fig. 24). Chan

does not disclose, for example, a Flash memory and SRAM formed on the same chip. Thus, Applicants submit that Chan does not teach or suggest a chip having a single common substrate.

For the above reasons, Applicants request that the rejection be reconsidered and withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert Downs Reg. No. 48,222 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

By _____

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